

## II-6. WIDEBAND VARACTOR HARMONIC MULTIPLIERS

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The basic circuit criteria for designing efficient narrowband harmonic multipliers are well established. For the case of the shunt-connected diode, ideal filters are usually specified that pass desired harmonics, reject others by having an infinite input impedance, and provide zero impedance paths for idler harmonics. As the bandwidth of allowable input frequencies is increased, it is desirable to maintain these ideal conditions. The stopband input impedance of most filters is entirely reactive and must change continuously with frequency. Since the ideal filter conditions call for the input impedance to be either infinite or zero, the optimum conditions can be obtained only at discrete frequencies. As in any practical situation, the ideal conditions can be approximated but, in general, bandwidths in excess of 10 percent become difficult to achieve. A common procedure for obtaining wider bandwidths is to use bandpass filters that have sharp cutoff characteristics. This guarantees that the real part of the stopband input impedance is small, but does not provide the ideal input conditions required. In fact, for most designs, interaction between the filter input impedances results in undesirable loading of the varactor and is a bandwidth-limiting factor.

In order to achieve wideband operation, it becomes apparent that the ideal filter conditions must be compromised. This should be accomplished in a manner that does not significantly reduce the obtainable efficiency. The two primary objectives in wideband multiplier design are (1) obtaining appropriate filter networks that do not adversely load the varactor and (2) designing matching networks that reduce the effect of varactor parasitic elements and impedance variation with frequency.

Before proceeding with a description of a circuit that accomplishes the above objectives, a number of important points will be discussed. First, only doublers will be considered. Higher order multipliers require low loss idler circuits for efficient operation, and these idlers are subject to the input impedance restrictions discussed previously. In general, the use of a number of wideband idler and matching circuits leads to very complicated network configurations. Second, only networks involving a single varactor will be considered. Various circuit configurations involving more than one varactor offer the possibility of wideband operation, but are usually difficult to realize at microwave frequencies. Third, the maximum spurious-free bandwidth for single varactor doublers is 40 percent. This arises from the fact that, for a 40 percent bandwidth, the third harmonic of the lowest input frequency is the same as the second harmonic of the highest input frequency. For wider bandwidths, spurious outputs will be obtained due to direct generation of the third harmonic. If this third harmonic can be tolerated, the maximum bandwidth becomes 2:1 or 67 percent.

A circuit that has been used to achieve wideband harmonic doubling consists of a complementary or pseudo-complementary (Reference 1) filter pair and associated matching networks. The configuration contains two parallel-connected filters whose common input is well matched over theoretically infinite bandwidths. The particular filters used are constructed of distributed quarter wavelength lines and are designed on an exact basis (References 1 through 3). A diagram of the circuit is shown in Figure 1. If the filters are constructed using line lengths that are a quarter wavelength at the input frequency, the network has the property that all odd harmonics pass through the input filter and all

even harmonics pass through the output filter.\* If constructed using quarter wavelengths at the output frequency, the input filter passes all harmonics but the 2nd, 6th, 10th, etc. The complementary filter pair provides a constant load for the varactor and thus eliminates undesirable filter interaction. This constant load property also results in a decrease in efficiency due to the loss of any power generated at higher harmonic frequencies. However, analysis and experimentation has shown that the amplitude of directly generated harmonics drops rapidly for harmonic numbers greater than two and the absence of low-loss idler paths tends to keep higher harmonic generation to a minimum. If very high spurious rejection is required, relatively simple complementary filter pairs can be added at the multiplier input and output ports to eliminate the unwanted harmonics. A suitable matching network is used between the filter pair input and the varactor to obtain a low input VSWR. For very wide bandwidths, additional matching networks can also be used at the input and output ports.

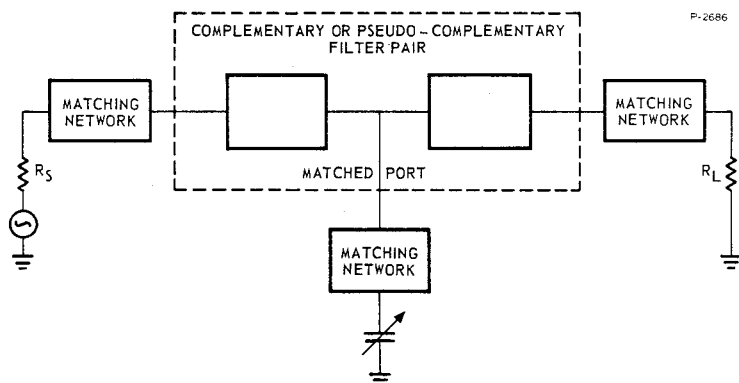


Figure 1. Block Diagram of Wideband Multiplier Circuitry

Using the network configuration described, an S-band to C-band doubler having a 20 percent bandwidth was constructed. Preliminary calculations indicated that the diode impedance would be approximately 10 ohms resistive and would contain a series capacitive reactive component. A quarter-wave transformer was used as a matching network. The performance characteristics are shown in Figure 2 and the multiplier is shown in Figure 3. The multiplier has an average efficiency of 50 percent, an output flat to within  $\pm 0.5$  db, and an input VSWR of less than 1.6 throughout the band.

\*This is a consequence of the periodic response of distributed quarter-wave TEM lines.

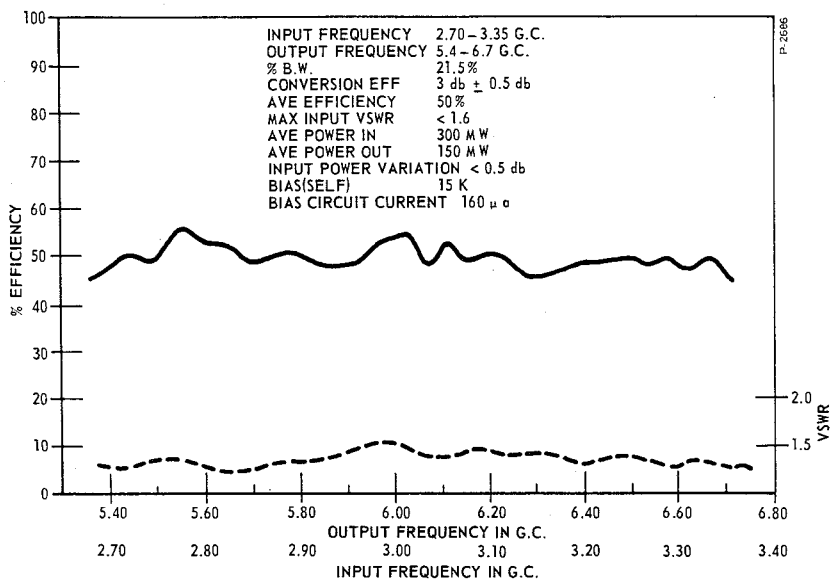


Figure 2. Twenty Percent Bandwidth Doubler Characteristics

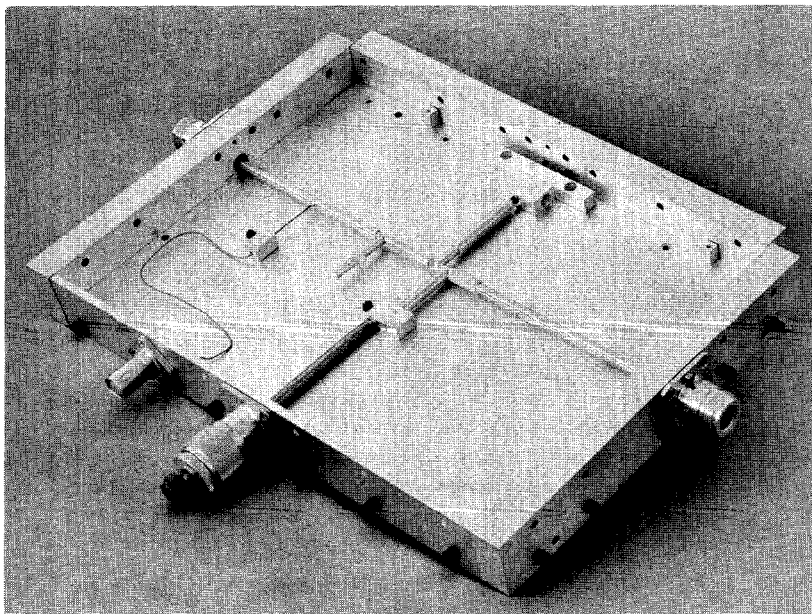


Figure 3. S-Band to C-Band Multiplier with 20 Percent Bandwidth

Another multiplier was constructed using a more complicated filter pair (Reference 3). Matching was accomplished in a manner similar to that described above with the addition of a section of lower impedance line on the input port. The performance characteristics over a 35 percent band are shown in Figure 4 and the unit is shown in Figure 5. The multiplier has an average efficiency of 43 percent, an output flat to within  $\pm 0.75$  db, and a maximum input VSWR of 1.6.

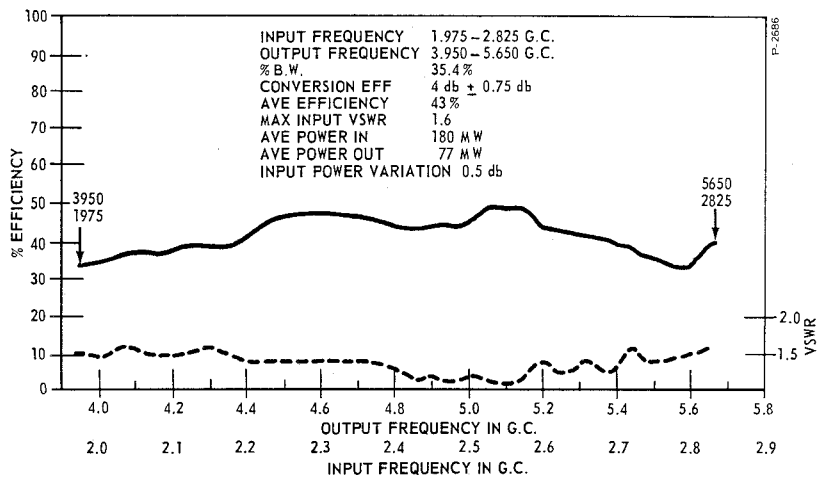


Figure 4. Thirty-Five Percent Bandwidth Doubler Characteristics

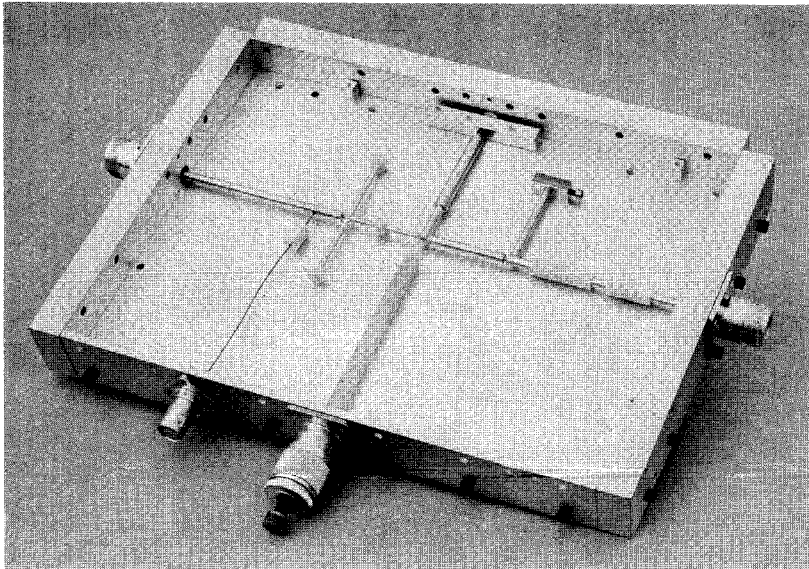


Figure 5. S-Band to C-Band Multiplier with 35 Percent Bandwidth

The efficiencies obtained in each multiplier compare favorably with those to be expected for narrowband designs, and similar performance was obtained for input power levels of from 100 mw to 800 mw. Self bias was used for input power levels below 400 mw with fixed bias being required for higher input power levels. Different varactors of similar types were substituted with no circuit adjustment\* and with almost identical results.

Multipliers of the type described are useful in obtaining high deviation wideband FM signals, wideband local oscillators, and in the extension of the frequency range of test equipment.

#### REFERENCES

1. Wenzel, R. J., "Application of Exact Synthesis Methods to Multichannel Filter Design," to be published in IEEE Transactions on Microwave Theory and Techniques, November 1964, or January 1965, presented at 1964 PTGMTT International Symposium, New York, New York.
2. Wenzel, R. J., "Exact Design of TEM Microwave Networks Using Quarter-Wave Lines," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-12, pp. 94-111, January 1964.
3. Horton, M. C. and Wenzel, R. J., "General Theory of Optimum Multipole Quarter-Wave TEM Filters," submitted for publication to IEEE Transactions on Microwave Theory and Techniques.

\*At high input power levels, a slight adjustment of the fixed bias voltage is usually required to obtain the best performance.

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